

Experiment SuperB at Cabibbo Lab.

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1. Introduction

The SuperB experiment [1] is an approved high luminosity flavour physics experiment that will perform detailed studies of the decays of B, D, Υ mesons and τ leptons with billions of events. Using these events it will be possible to start reconstructing the Lagrangian for any physics beyond the Standard Model that may be encountered, and precise tests of the Standard Model of particle physics. The experiment will be built at the newly created Cabibbo Laboratory in Tor Vergata (Rome).

The contribution of the Lecce group is concentrated on the implementation of the Cluster Counting/Timing methodology to the readout of the drift chamber of the SuperB apparatus.

The drift chamber (DCH) is the main tracking and momentum-measuring system. It provides precision momentum measurements, as well as good particle identification for low momentum tracks (those below DIRC threshold) and for tracks in the forward direction, outside the DIRC acceptance. The DCH design is based on the BABAR drift chamber, described in detail in the original BABAR detector publication [2].

2. Drift Chambers Fast Readout Cluster Counting/Timing algorithm implementation and test on a FPGA Board

A fast readout algorithm [3,4] for Cluster Counting and Timing purposes has been implemented and tested on a Virtex 6 core FPGA board. The algorithm analyzes and stores data coming from a Helium based drift tube instrumented by 1 Gsample/s ADC; the algorithm represents the outcome of balancing between efficiency and high speed performances, resulting in high efficiency peak data extraction on simulated signals as well as on experimental ones. A relative efficiency evaluation using commercial peak finder software (i.e. PeakFit) has been carried out too (shown in Fig.1). Based on last results, the developed algorithm (described in Fig.2) can be

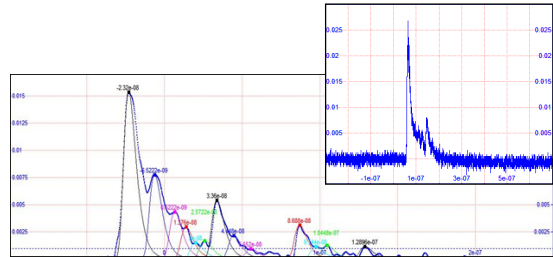
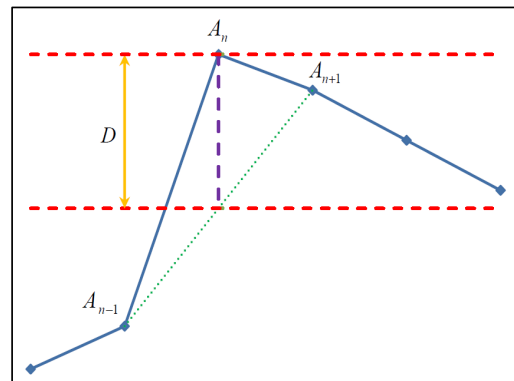


Figure 1. Reconstructed peaks in a typical pulse (in the inset) generated by a m.i.p. in a drift tube, 8mm diameter, 90%He – 10% iC_4H_{10} , gas gain 10^5 , sampled with a 8GHz, 12GSa/s, 8bit oscilloscope. In these conditions, one expects of the order of 10 clusters total.



$$D = A_n - \left(\frac{A_{n-1} + A_{n+1}}{2} \right) \geq 3\sigma_d$$

$$\sigma_d^2 = \sigma_{A_n}^2 + \frac{1}{4}\sigma_{A_{n-1}}^2 + \frac{1}{4}\sigma_{A_{n+1}}^2 = \frac{3}{2}\sigma^2$$

Figure 2. A brief description of the fast numeric algorithm developed for the FPGA.

adopted in order to build a VME electronic board that should serve, initially, at least 4 fADC channels and it can be used as on-line preprocessing stage for signals coming from the SuperB DCH.

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