A CMOS high-speed Variable Gain Amplifier for Cluster Counting Technique in Ionization Detectors

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The counting of the consecutive ionization clusters in a drift chamber is a very promising technique for particle identification purposes. Although this technique features a number of advantages, the bottleneck for its implementation is represented by the difficulties in realizing a low cost, small area occupancy, low-power consumption, high-speed electronic interface.

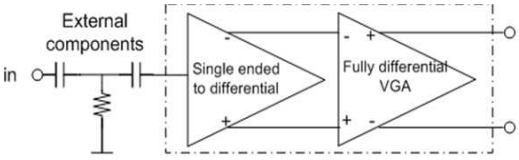

Figure 1. The VGA architecture.

Typical time separation between each ionization act in a helium-based gas mixture is from a few ns to a few tens of ns. Thus the read-out interface has to be able to process such a high-speed signals. Starting form these considerations, an integrated circuit solution seems to better fit these requirements.

We developed a CMOS 0.13 μm integrated readout circuit, including a fast Variable Gain amplifier (VGA), with a -3 dB bandwidth of 160 MHz and three gain steps (0 dB, 10 dB, 20 dB) is presented [1],[2].

The proposed VGA presents characteristics of very low current consumption (10.6 mA at 20 dB gain setting). Moreover, the current consumption is adjusted according to the selected gain setting.

The VGA block diagram is reported in Figure 1. The external RC network guarantees an AC coupling and input matching. The VGA presents a fully differential architecture in order to be more robust against disturbs from supply. The signal coming from the drift tube is single-ended. Therefore, a single-ended to differential stage is mandatory. This stage is followed by a differential variable gain amplifier. The first stage is simple because it should guarantees high frequency of working and low power consumption.

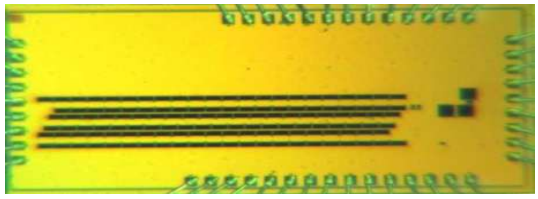

Figure 2. The VLSI chip micro-photograph.

The gain is set by reconfiguring the amplifier input stage. This allows to obtain an almost about constant bandwidth an a power consumption. optimization.

The baseband receiver chain has been realized in a 0.13 μm CMOS technology with 1.2 V supply voltage. The active die size occupancy is 260 μm x 260 μm and the VLSI chip micro-photograph is reported in Figure2.

The several circuital blocks were designed and simulated by Cadence 5.05 CAD and Matlab 7.0.0 . In order to meet the UMC foundry schedule we didn't do the post-layout simulation necessary to extract the parasitic elements.

We realized a test circuit board with four copper layers, in order to test and characterize the chip on the bench.

Figure 3 shows the VGA frequency behavior for the three gain settings. The VGA cut-off frequency is 160 MHz at 0 dB and 10 dB gain settings, and 140 MHz at 20 dB gain setting.

Figure 4 shows the output noise spectral density for 20 dB gain setting. At 100 MHz the Output noise level is -132 dBm.

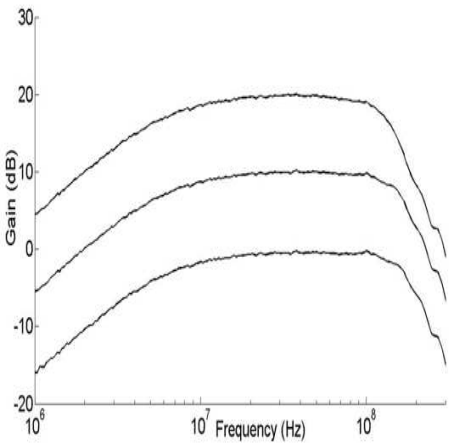

Figure 3. Frequency response for different gain settings.

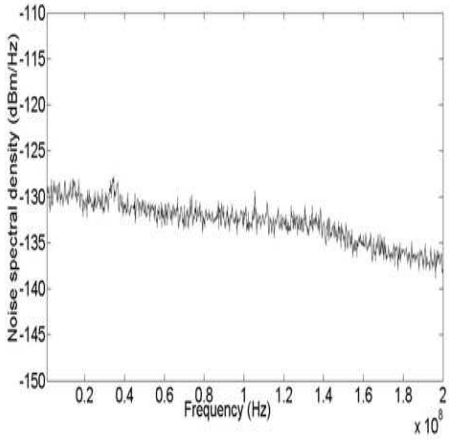

Figure 4. Output noise spectral density.

The Total Harmonic Distortion (THD) is reported in Figure 5 as a function of the output signal level. A 10 MHz input sine frequency has been applied. At 0 dB gain setting and 0 dBm output signal level, the THD is -36 dB. The current consumption depends on the gain setting. It goes from 8.4 mA at 0 dB gain setting up to 10.6 mA at 20 dB gain setting, well below the power budget limit of about 20 mW per channel assigned to the analog part.

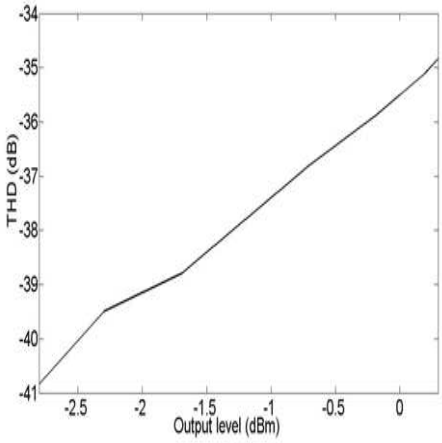

Figure 5. THD vs. output signal level.

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1. A. Baschirotto, S. D'Amico, M. De Matteis, F. Grancagnolo, M. Panareo, R. Perrino, G. Chiodini, G.Tassielli. "A CMOS high-speed front-end for cluster counting techniques in ionization detectors." Proceeding of IWASI 2007.
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