



Final Data Format Description of the RPC Detector of the Muon System

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Abstract

The Resistive Plate Chamber (RPC) detector will act as trigger detector for the Muon Spectrometer. The Muon LVL1 Trigger Electronics will not only generate and transfer the trigger relevant data to the trigger chain, but will also route the data coming from RPC front-end electronic to the RPC ReadOut Driver (ROD) that will then push them in the ATLAS DAQ data flow. Here the data format of the RPC system from Coincidence Matrix ASIC up to the ROD will be described.

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1 INTRODUCTION

This note presents the RPC data format that is used by the readout system of this detector. The data structure reflects the architecture of the barrel LVL1 muon trigger [1] system that is indeed based on RPCs. Information on the geometry of the RPC system is available in [2].

The RPCs are strip detectors with time resolution $\sigma_t = 1.5$ ns; the typical strip size is 3 cm. The trigger is based on three stations. Two stations are used for low-pT triggers, while the third station is used in addition for high-pT triggers. Each station is composed of two detector planes and each detector plane is read out in two orthogonal projections, η and ϕ . The RPC system is important also for high-level trigger algorithms and offline muon reconstruction program because it provides the measurement of the second coordinate of muon trajectories.

2 THE BARREL LEVEL-1 MUON TRIGGER SYSTEM

The signals from the RPC detector are amplified, discriminated and digitally shaped on the detector. The Amplifier-Shaper-Discriminator (ASD) boards are attached to the chamber at the end of the RPC strips. In the low-pT trigger, for each of the η and ϕ projections, the RPC signals of the first two RPC stations are sent to a Coincidence Matrix board (CM), whose core is the CM chip. This chip performs almost all of the functions needed for the trigger algorithm and also for the readout of the RPC strips. The CM board produces an output pattern containing the low-pT results for each pair of RPC doublets in the η or ϕ projection. Moreover, the highest thresholds satisfied by the trigger conditions and a flag indicating triggers occurring in regions of overlapping RPCs are also provided. The information of two adjacent CM boards in the η projection, and the corresponding information of the two CM boards in the ϕ projection, are combined together in the low-pT Pad Logic board. Each Pad board hosts globally 4 CMs. In the high-pT trigger, for each of the η and ϕ projections, the RPC signals of the third station, and the corresponding pattern result of the low-pT trigger, are sent to a CM board, very similar to the one used in the low-pT trigger. The information of two adjacent CM boards in the η projection, and the corresponding information of the two CM boards in the ϕ projection, are combined together in the high-pT Pad Logic board. Again, each Pad board hosts 4 CMs. The high-pT Pad board combines the low- and the high-pT trigger results. The combined information is sent to a Sector Logic (SL) board, located in the USA15 counting room.

3 THE RPC DATA FORMAT

3.1 The Read-Out scheme

The whole RPC barrel trigger system is read-out by 32 RODs. The ROD collects the information, of both middle and outer chambers, of two adjacent half-barrel large octants. The ROD will be located in the USA15 underground counting room.

The format structure of the RPC data is based on the fragment provided by the CM boards. Here the fired RPC strips, the trigger output and the highest threshold satisfied by the trigger logic, as well as the overlap flag, are reported. The fragments of (up to) eight CMs belonging a given Pad board (4 low-pT CMs plus 4 low-pT CMs) are written out one after the other, adding a header/footer at the beginning/end of this list. This is a Pad fragment.

Similarly, the fragments of the Pad belonging a given Sector are written out one after the other, adding a header/footer at the beginning/end of this list. This makes the RX fragment. Finally, two adjacent RX fragments belonging to the same half-barrel trigger system are put together and form the ROD fragment.

3.2 The CM fragment

The CM fragment structure is shown Figure 3-1

CM Frame

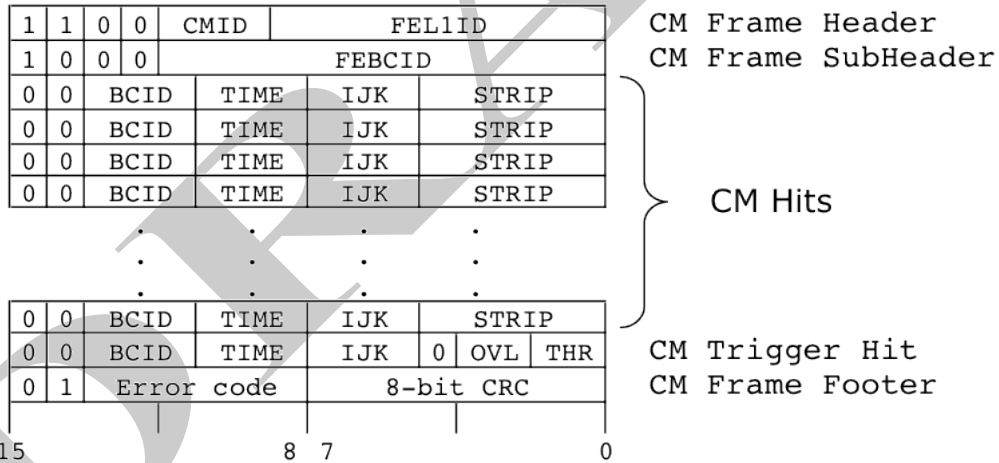


Figure 3-1: The scheme of the Coincidence Matrix read-out fragment (see text)

The 16-bits data word are framed in a block starting with an header, followed by a sub-header, a body block that collects the RPC hits and the trigger output, and finally a footer. The header is identified by the 4-bit sequence “1100” from bit 15 to 12 (from here onwards bits are counted starting from 0). This word contains the identifier of the CM board (CM-ID) and the bunch crossing identifier from the Level-1 Electronics. The CM-ID is a 3-bit word packing information according to Table 3-1.

The sub-header word is identified by the 4-bit sequence “1000” from bit 15 to 12. It contains the bunch crossing identifier from the Front-End Electronics.

Following the sub-header there are the RPC hits and the trigger output words identified by the 2-bit sequence “00” from bit 15 to 14.

	<i>Bit 2</i>	<i>Bit 1</i>	<i>Bit 0</i>
<i>0</i>	<i>Low p_T CM</i>	<i>φ projection</i>	<i>Address of 1st CM</i>
<i>1</i>	<i>High p_T CM</i>	<i>η projection</i>	<i>Address of 2nd CM</i>

Table 3-1: The CM identifier scheme

For each RPC fired strips, named here hit, the following 4 field are packed in a 14-bits word: the BCID containing the bunch crossing id; the TIME containing the interpolatore clock time, the IJK coding RPC layer and station, and the STRIP containing the CM channel number connected to the fired RPC strip. BCID and TIME give the time coordinate of the given hit. The IJK identifiers are described in Table 3-1.

<i>IJK</i>	<i>Layer & Station</i>
0	<i>Pivot Station, Layer 0</i>
1	<i>Pivot Station, Layer 1</i>
2	<i>Confirm Station, Layer 0, Chan 0-31</i>
3	<i>Confirm Station, Layer 0, Chan 32-63</i>
4	<i>Confirm Station, Layer 1, Chan 0-31</i>
5	<i>Confirm Station, Layer 1, Chan 32-63</i>
6	<i>Trigger Pattern</i>
7	<i>Highest Threshold & Overlap</i>

Table 3-2: Description of the IJK identifier

All these hits are ordered following increasing first values of IJK (up to IJK=6), then of BCID, TIME and STRIP.

In case of trigger, additional words are added: first the strip of the pivot plane that provided the trigger itself, and then an additional word where the STRIP identifier is replaced by the identifier THR representing the highest threshold satisfied by the trigger logic, and the overlap flag OVL.

THR can range from 1 to 3. The OVL flag is described in Table 3-3

Finally, the CM fragment is completed by the footer word; this word is identified by a 2-bit pattern “01” from bit 15 to 14. It contains the CRC calculated using all the data present in the CM fragment in the lowest 7 bits and a 6-bit wide word coding errors starting at bit 13. The meaning of each of the 6 bits is reported in

Then a fragment for each CM is inserted; these fragments are ordered with increasing values of CMID and in order to transmit FEBCID (Front-End Bunch Crossing ID) and FEL1ID (Front-End Level-1 ID) one CM is anyway present.

After the CM fragments a pre-footer word is present, identified by the 4-bit sequence “1010” which in the lower 12 bits has a PAD status word which is described in Table 3-1.

The footer word, containing error codes described in Table 3-6, completes the PAD fragment and it is identified with the bit pattern “0111” from bit 15 to 12

Bit Position	Bit coding	Flag when set to 1
0÷7	CM busy pattern	Each bit represent a CM busy
8	OR XOFF fifo CM	At least one CM fifo on PAD is FULL
9	XOFF fifo L1	PAD L1 fifo is FULL
10	XOFF fifo PAD	At least one busy flag (CM or L1)
11	OR busy CM	At least one CM is busy

Table 3-5: Detailed description of PAD Status word (CM are identified by their CMID)

The PAD Footer contains some error code for debugging purpose:

Bit Position	Bit coding	Flag when set to 1
0÷7	CM error pattern	1 bit per CM where an error occurred
8	CM Error	At least 1 CM is missing
9	Header Error	At least 1 CM Header is missing
10	L1 Error	At least one Level -1 ID misaligned
11	Subheader Error	At least one subheader is missing

Table 3-6: Detailed description of PAD error word

3.4 The RX fragment

The RX fragment collects the Pad data belonging to a given logic sector. Its scheme is illustrated in Figure 3-3. The header word is identified by the bit pattern “1001” from bit 15 to 12. The RX header word contains the RX identifier (starting from 0) and the status bits. Up to 8 PAD frames, belonging to the same sector logic, are then appended below in ordered way, following the increasing value of PADID.

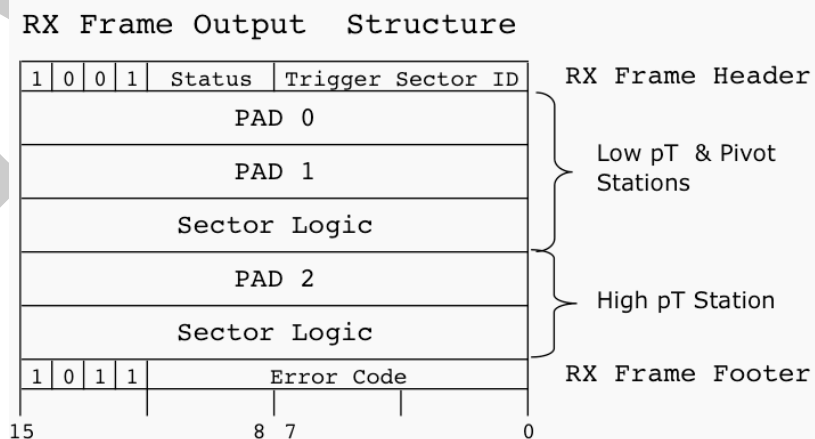


Figure 3-3: Scheme of the RX readout fragment

At least one Pad fragment is always reported to transmit FEL1ID and FEBCID.

A further block of data can be appended for debugging purpose. This block of data contains the Sector Logic information which are redundant to the ones already present and allows to cross check the LVL1 functioning. A description of the block of data will be given in appendix A.

Finally, the footer word, identified by the bit pattern “1011” from bit 15 to 12, is added and it contains error flags.

3.5 The ROD fragment

The general format of the ROD fragment of ATLAS is reported in details in [3]. The size of the ROD fragment word is 32 bits. The 16-bit RX words are copied in the “Data Elements” region of the ROD fragment starting from bit-0.

4 REFERENCES

- [1] ATLAS First-Level Trigger Technical Design Report, CERN/LHCC/98-14.
- [2] <http://atlas.web.cern.ch/Atlas/GROUPS/MUON/layout.html>
- [3] C. Bee et al., “The raw event format in the ATLAS Trigger & DAQ”, Atlas Technical Note ATL-DAQ-98-129, October 2002.

DRAFT

5 APPENDIX A

5.1 The RPC data word identifier

The table below summarizes all the 4-bit word used to identify RPC data in the field from 15 to 12.

<i>hex code</i>	<i>Bit 15</i>	<i>Bit 14</i>	<i>Bit 13</i>	<i>Bit 12</i>	<i>Data Word Type</i>
0x0/0x3	0	0	x	x	<i>CM Hit</i>
----	0	1	x	x	<i>CM Footer</i>
0x5	0	1	0	1	<i>PAD Header</i>
0x6	0	1	1	0	<i>PAD Subheader</i>
0x7	0	1	1	1	<i>PAD Footer</i>
0x8	1	0	0	0	<i>CM Subheader</i>
0x9	1	0	0	1	<i>RX Header</i>
0xA	1	0	1	0	<i>PAD Prefooter</i>
0xB	1	0	1	1	<i>RX Footer</i>
0xC	1	1	0	0	<i>CM Header</i>
0xD	1	1	0	1	<i>SL Header</i>
0xE	1	1	1	0	<i>SL Trigger Hits[†]</i>
0xF	1	1	1	1	<i>SL Footer</i>

Figure 5-1: Hexadecimal and binary code for data control word

[†] This will be true only for the final RX board, but is not yet implemented.

5.2 The Sector Logic Frame

Here we will give a brief description of the information available in the Sector Logic frame shown in Figure 5-2

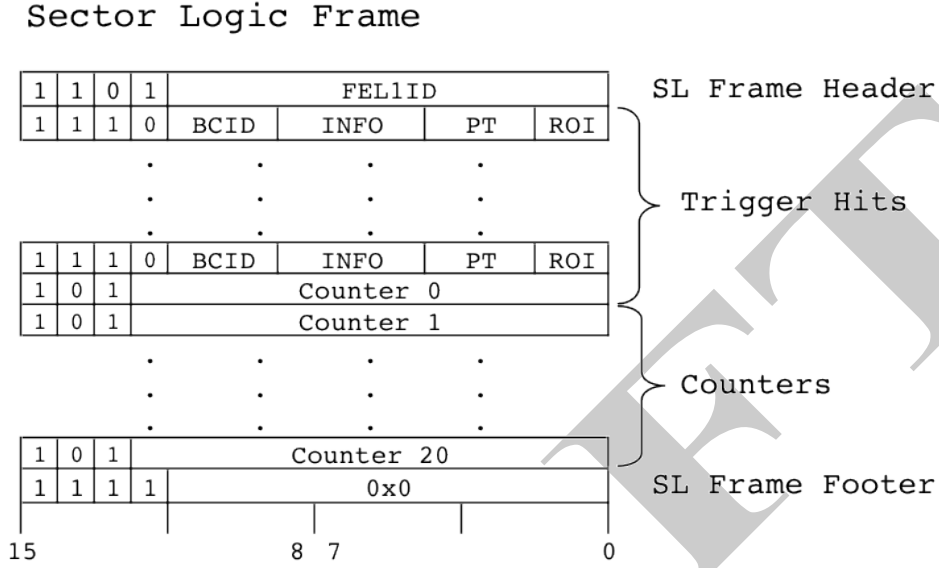


Figure 5-2: Scheme of the Sector Logic Frame

The frame start with a header, identified by the 4-bit binary sequence “1101” from bit 15 to 12, containing the FEL1ID; it then follows the the trigger hits and afterward a series of counter are included.

In the final board[†] the trigger hits will be identified by the 4-bit binary sequence “1110”; they pack together four fields: the BCID, the pT threshold, the ROI Region of Interested, and an INFO 4-bit word packing some relevant bit. detail is shown

The INFO field further packs 4 bits:

- **OPL** (Outer Plane Flag) in some case for low pT muons an high pT plane is used as confirmation for the low pT trigger
- **OVF** (Overlap Phi) This bits flags an overlapping hits in the φ direction
- **OVE** (Overlap Eta) This bits flags an overlapping hits in the η direction
- **RES** (reserved)

These trigger hits are ordered according to the increasing bunch-crossing number, ranging from 0 to 6; the trigger hits belonging to the same bunch-crossing are collected from all the PAD (up to maximum of), so that hits belonging to the same PAD but to different bunch crossing are not found one next the other.

[†] For the current configuration the trigger hits do not have a defined 4-bit pattern in the control bit 15 to 12

†The Sector Logic has 7 counters, each packed in three 13-bit wide words for a total of 21 counter word (see Figure 3-3); in Table 5-1: Content of the Sector Logic countersTable 5-1 the content of each counter is reported.

COUNTER 1	<i>pad 0 trigger data enable 0</i>
COUNTER 2	<i>pad 0 trigger data enable 1</i>
COUNTER 3	<i>pad 1 trigger data enable 0</i>
COUNTER 4	<i>pad 1 trigger data enable 1</i>
COUNTER 5	<i>sector logic valid trigger</i>
COUNTER 6	<i>selected Level-1 accept</i>
COUNTER 7	<i>lost Level-1 accept</i>

Table 5-1: Content of the Sector Logic counters

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† This counters are present for debugging purpose and then their size and content can undergo major changes in future chipset revision.

APPENDIX B

5.3 The data format for the cosmic setup (Sector 13)

The data format described up to now all along this note is the final one to be used in the ATLAS normal running operation. During the actual phase, in which was decided to operate a half of the already installed sector 13, not all the electronic is in the final shape.

This is not relevant at this stage because the driving goal is to integrate and operate, detector, trigger and DAQ on a real set-up using real data coming from cosmic going through.

Moreover due to the fact that the sector is nor fully installed nor fully equipped, the number of PAD, the Sector Logic and more in general the data and their format cannot be like the final one. It is anyway very important in order to debug and understand the system to play a full scale exercise on this first real data: to this aim a description of the actual data format will be given here.

In the actual setup only 2 half trigger sector are installed and equipped in sector 13; this means that 6 PAD are present, 3 for each of the two sectors.

It is obvious that some PAD fragment are missing in the RX frame: moreover it was chosen to have a different RX framing reflecting the current hardware set-up and helpful for debugging.

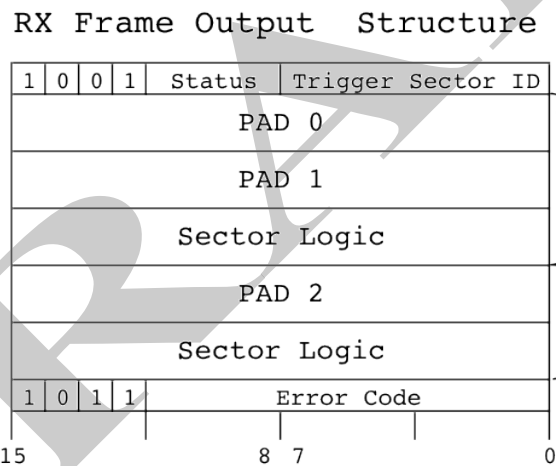


Figure 0-1: RX Frame in the Sector 13 set-up