LECCE - DAQ PER ITK-PIXEL

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GOALS

- General:
  - We are a half-ring loading site => in production mode we need to be able to
    - Perform module reception tests (electrical and visual)
    - Perform electrical multi-module tests post-loading
      - with DAQ/DCS for typical system-tests (a la SR1 and integration tests)
      - Cooling via half-ring cooling system => CO2 based - Marta
      - With serial powering
        - Before/after thermal cycling the loaded half-ring (subject to the definition of the ATLAS wide QC procedures
    - Get and store data of all component to ATLAS production DB

- On the time scale of the local support FDR (Fall 2022):
  - We aim to demonstrate the ability of testing (a few digital) modules loaded on a prototype local support, hosted in the test-transport box (as ready for shipping to the integration site) exercising DAQ/DCS/Cooling/Interaction with DB as in “production mode” (i.e. demonstrating readiness of all needed infrastructures)

What we did so far

- In Feb 2020, we took part in the traveling chip pixel-wide exercise:
  - Lecce report (on chip 3, 0x495) is linked at the corresponding entry here: https://twiki.cern.ch/twiki/bin/viewauth/Atlas/ContactDetails

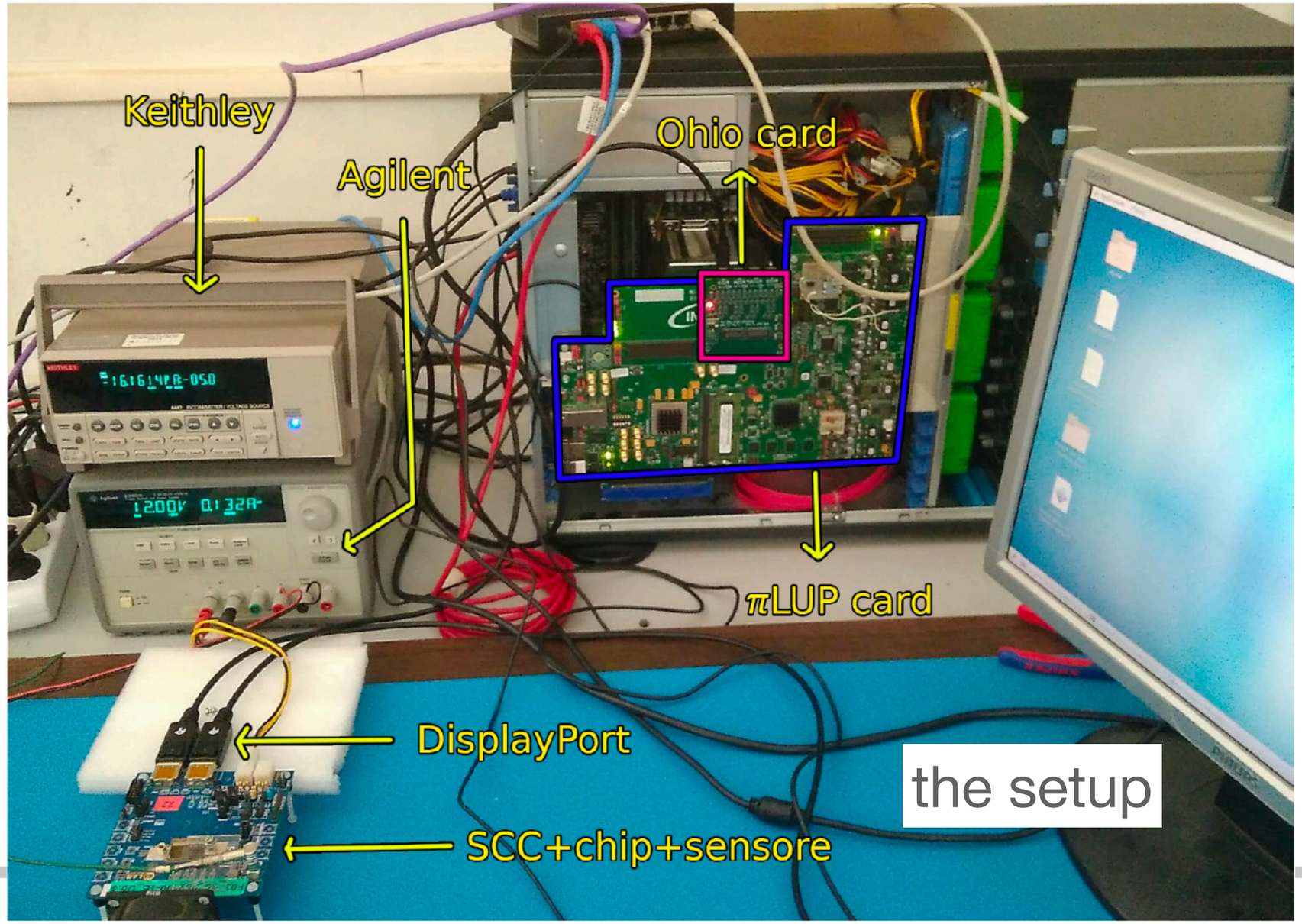
The setup consists in

1) DAQ board: πLUP, developed for TDAQ studies in BO (A. Gabrielli et al) instead of the typical YARR board, but featuring the same FPGA and general features; it requires a slightly modified firmware w.r.t. typical fw of YARR setup (thanks to K. Naoki)

2) SCC

3) DAQ sw YARR

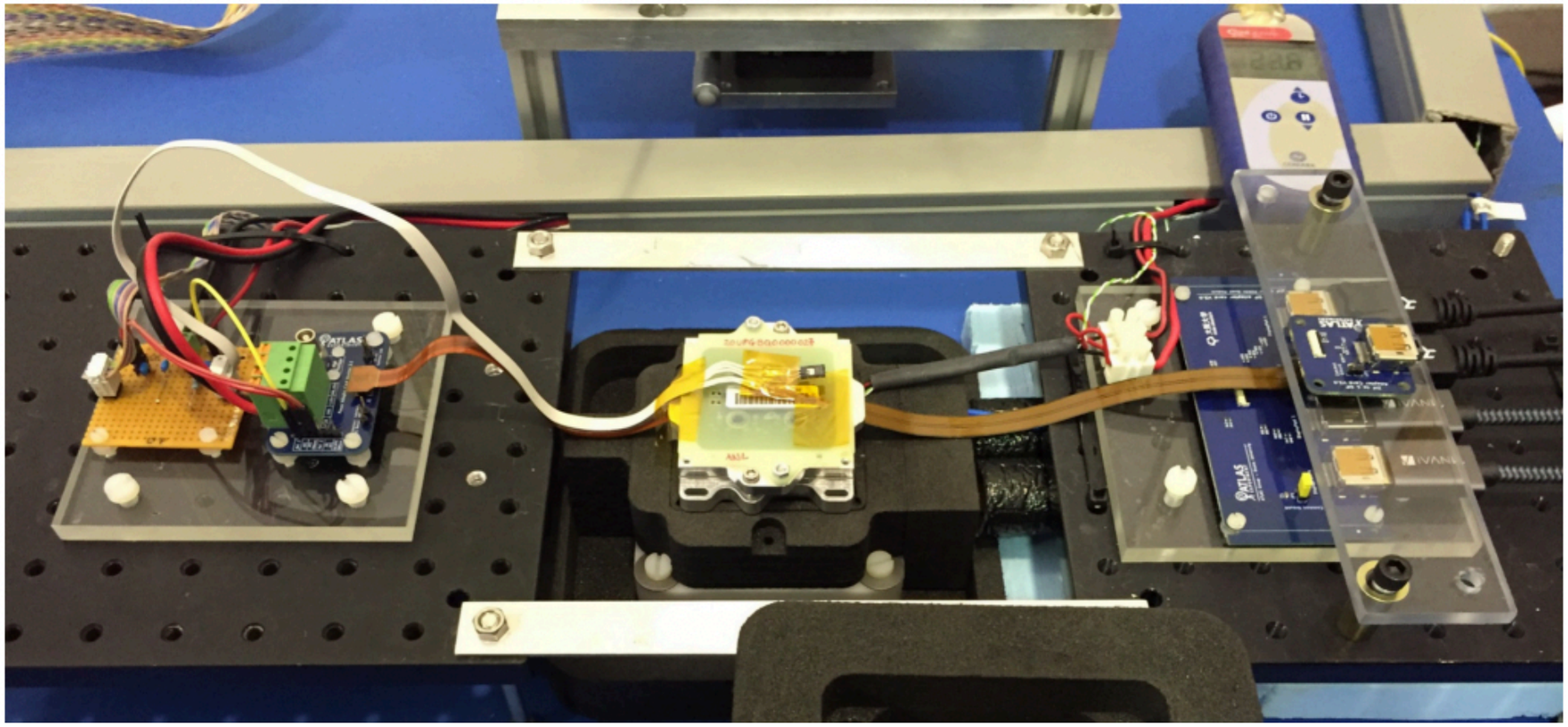
4) Standard LV power supplies and Picometer



the setup

WHAT WE DID SO FAR

- June 1st 2021, Lecce (as loading site) qualified for the module reception tests presenting results of tests on a digital module (link to the slides: https://indico.cern.ch/event/1044649/contributions/4389089/attachments/2256176/3828386/2021-05-25_digitalQuad_testLecce.pdf)
  - In practice demonstrating the same ability of performing electrical tests as module production site (same equipment)



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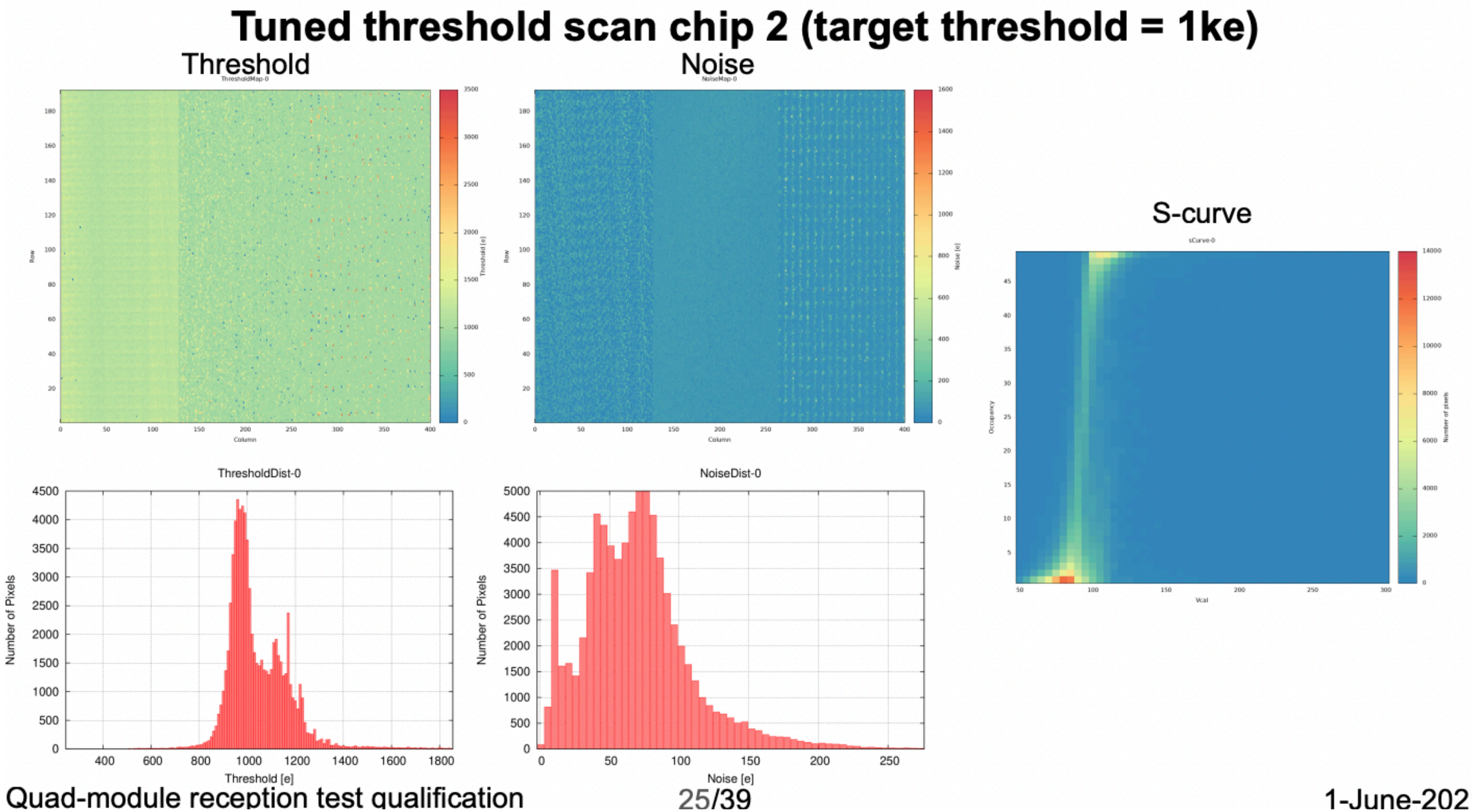
  - In practice demonstrating the same ability of performing electrical tests as module production site
  - we were provided the same test equipment as module production sites):
    - A digital quad module + interface card for 4chip data to DAQ + power distribution + temperature sensing card
- We used the same DAQ system (πLUP based), YARR software and we exercised access to the production DB / writing to the local DB
- DCS (see Gabriele slides)
- Successful scan (digital, analog, threshold, noise) and tuning (threshold & time over threshold) of all 4 chips

WHAT WE DID SO FAR

Some example plot

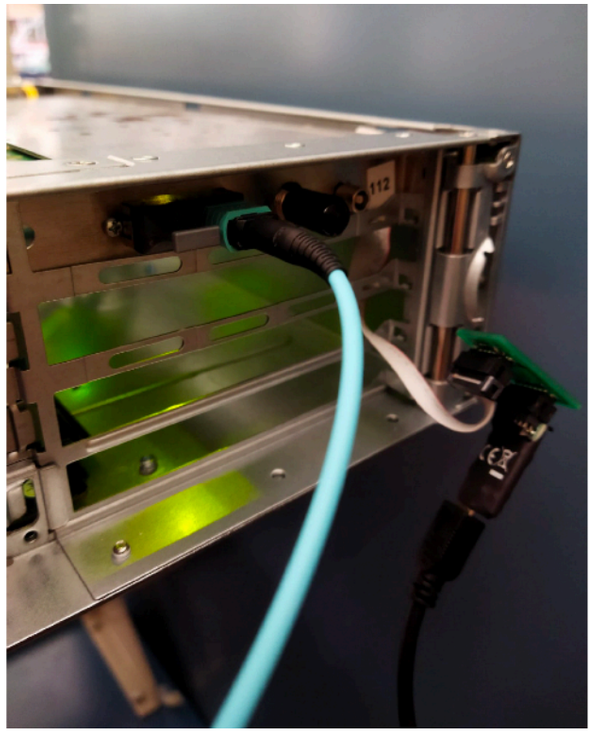


THESE DAYS

- Moving electrical tests to a Felix-based setup

to be replaced by optobox in the near feature

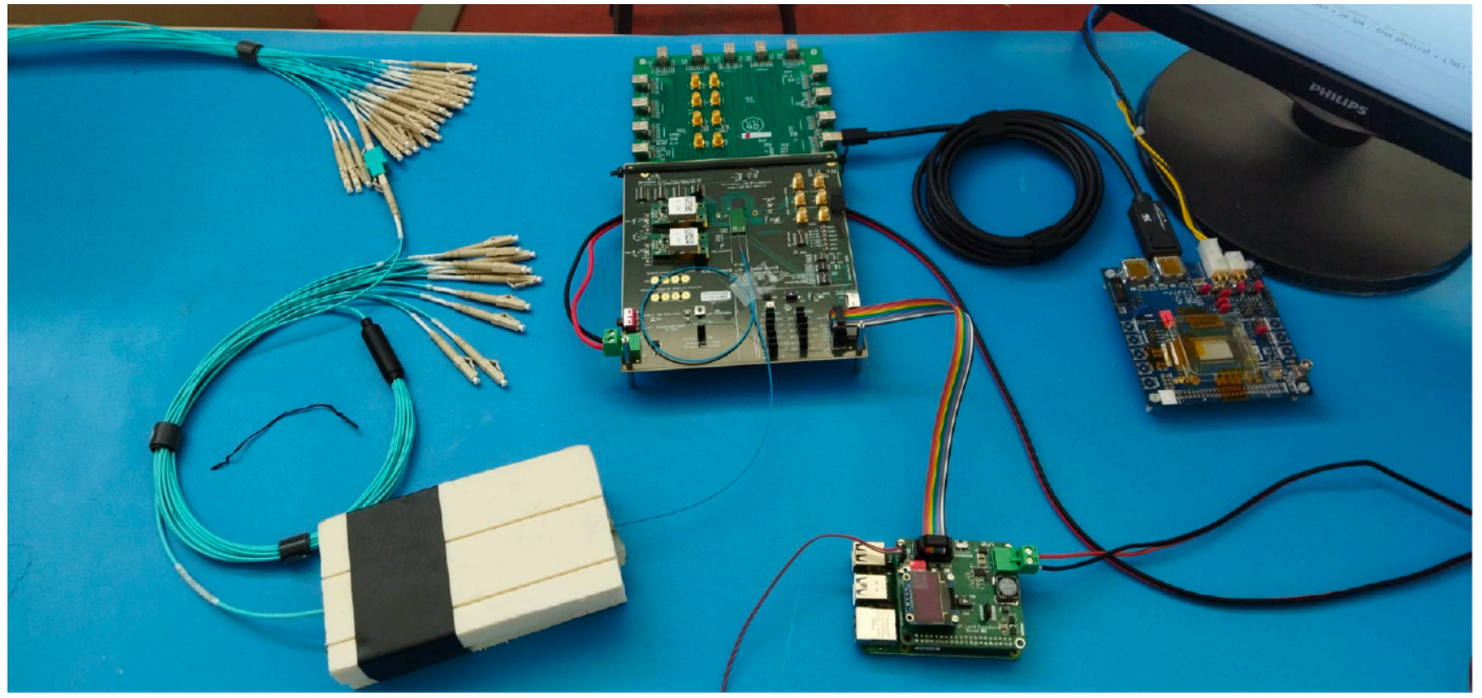
Server with FLX712 board
24x MPO bundle



Optical fibers

Optical fibers to LpGBT
VLDB+ and its controller

Single chip card



- Felix code from TDAQ -> Felix core + Netio
- Readout DAQ
  - Yarr
  - Itk-felix-sw (TDAQ integrated): https://gitlab.cern.ch/itk-felix-sw/RD53Emulator
    - In fast evolution

Apparently everything ready to run scan procedures, but not yet pixel hits read back

Next steps - toward local support FDR

- Having the Felix setup working
  - And it's evolution with the optobox
- Integrating readout software with DB (done for module testing)
- Prepare for serial powering, as soon as prototype components are available
- Prepare for data transmission from module via production pigtails / interface cards
- Exercising DAQ / DCS communication:
  - Following starting effort of prototyping DDC following ATLAS design and (ITk pixel) requirements at SR1 (A. Palazzo + SR1 daq/dcs team)
    - See https://indico.cern.ch/event/1160515/contributions/4884423/attachments/2447974/4194837/DAQtoDCScommuncation_May20.pdf